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An analytical model for square GAA MOSFETs including quantum effects

E. Moreno [a], J.B. Roldán [a,*], F.G. Ruiz [a], D. Barrera [b], A. Godoy [a], F. Gámiz [a]

[a] Dpto. de Electrónica y Tecnología de los Computadores, Facultad de Ciencias, Universidad de Granada, 18071 Granada, Spain
[b] Dpto. de Matemática Aplicada, Facultad de Ciencias, Universidad de Granada, 18071 Granada, Spain

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ABSTRACT

In this paper we introduce an analytical model for square Gate-All-Around (GAA) MOSFETs including quantum effects. With the model developed, it is possible to provide an analytical description of the 2D inversion charge distribution function (ICDF) in square GAA MOSFETs of different sizes and for all the operational regimes. The accuracy of the model is verified by comparing the data with that obtained by means of a 2D numerical simulator that self-consistently solves the Poisson and Schrödinger equations. The expressions presented here are useful to achieve a good description of the physics of these transistors; in particular, of the quantization effects on the inversion charge. The analytical ICDF obtained is used to calculate important parameters from the device compact modeling viewpoint, such as the inversion charge centroid and the gate-to-channel capacitance, which are modeled for different device geometries and biases. The model presented accurately reproduces the simulation results for the devices under study and for different operational regimes.

1. Introduction

Multiple-gate (MuG) MOSFETs are considered a serious alternative for keeping up with the continuous reduction in device dimensions imposed by Moore's law. These structures show promising possibilities in relation to the control of short channel effects (SCEs) and the achievement of ideal subthreshold swing values [1–3].

Making use of technologies based on these new geometries, channel lengths could be shrunk to below 22 nm accordingly to the latest edition of ITRS [1]. In this respect, their capacity to reduce SCEs and the possibility of using undoped channels are essential features for the achievement of this goal. The latter, in particular, is critical since random impurity effects are by no means negligible in nanometric devices [4,5]. These effects produce a dispersion of fundamental parameters such as the threshold voltage and the subthreshold slope [4–7]. Moreover, MuG MOSFETs are part of the Silicon-On-Insulator (SOI) transistor family, which demonstrates unique features that look promising for future mainstream CMOS technologies [6,7]. The use of ultra-thin-body (UTB) and MuG SOI structures allows the fabrication of fully-depleted devices that offer not only extremely good control of SCEs but also a very good behavior with respect to drain-induced barrier-height lowering (DIBL), threshold voltage roll-off, and off-state leakage [6,7].

Both square and cylindrical Gate-All-Around (GAA) MOSFETs are currently under intense study from the simulation and modeling viewpoint [3,8–17]. One key area in these structures is the study of quantum mechanical effects (QMEs), since both structural and electrical confinement (produced by a square gate in the quadruple-gate device and by a circular gate in the cylindrical one) make these devices (nanowires FETs) quasi-1D transistors, where transport occurs in a set of loosely coupled propagating modes.

In this work we focus on square GAA MOSFETs. To the best of our knowledge, these devices have not previously been analytically described in any depth due to their particular geometrical complexities. The concentration of inversion charge close to the corners of the silicon body makes a bi-dimensional description of the inversion charge distribution and other important magnitudes imperative from the compact modeling viewpoint. The analytical description of cylindrical GAA MOSFETs is simpler since the symmetry of the structure around the rotation angle allows a 1D description, accounting for just the radial component [11,13,10,16]. In the case of square GAA MOSFETs, other modeling strategies are necessary.

First, we have introduced an analytical function $f(y,z)$ that accurately reproduces the inversion charge distribution function (ICDF) for square GAA MOSFETs of different sizes and for different biases. The ICDF is related to the inversion charge density as $n(y,z) = N_{inv}|f(y,z)|^2$, N_{inv} (cm^{-1}) being the value of the total electron density integrated over the square area of the silicon channel. Second, we have successfully modeled the inversion charge

* Corresponding author. Tel.: +34 958 244071; fax: +34 958 243230.
E-mail address: jroldan@ugr.es (J.B. Roldán).

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centroid (ICC) and the gate-to-channel capacitance (C_{GC}), making use of the proposed analytical ICDF. The geometry of these devices makes the definition and modeling of the ICC a tough issue. To deal with this, we have presented a definition that correctly characterizes the spatial distribution of the inversion charge in the silicon channel.

The paper is organized as follows: in Section 2 we describe the main features of the simulator used. We deal with the ICDF modeling in Section 3. The definition, calculation and modeling of the ICC and the C_{GC} are presented in Sections 4 and 5, respectively. Finally, the main conclusions are given in Section 6.

2. Simulator description

The simulation data presented in this work have been obtained by using a simulator developed within our research group [8,12]. The geometry and cross-section of the GAA MOSFET studied is shown in Fig. 1, where t_{ins} and t_{Si} are the insulator thickness and the silicon body thickness, respectively. It can be seen that the gate completely surrounds the square silicon channel where conduction takes place. To reach a fast convergence, the 2D Poisson and Schrödinger equations, the latter solved for each energy valley, have been self-consistently solved using the predictor-corrector scheme proposed by Trellakis et al. [18] including the energy valley degeneration of the silicon conduction band. The simulator achieves accurate results for different structures, materials and gate voltages if the number of energy levels and their corresponding wave functions employed in the calculation is high enough to capture all the occupied levels.

The geometry of the device shown in Fig. 1 confines the electrons in the plane perpendicular to the transport direction, which means that we are dealing with a 1D electron gas. The quantum charge density is therefore obtained by evaluating the following expression [8,18]:

$$\rho(y,z) = \frac{q}{\pi}\left(\frac{2mk_BT}{\hbar^2}\right)^{\frac{1}{2}} \sum_n \Psi_n^2(y,z)\Im_{-\frac{1}{2}}\left(\frac{E_F - E_n}{k_BT}\right)\left[\frac{C}{cm^3}\right] \quad (1)$$

where q is the electron charge, E_F is the Fermi level, Ψ_n is the wave function belonging to energy level E_n, $\Im_{-1/2}$ the complete Fermi–Dirac integral of order $-1/2$ and the remaining symbols have their usual meaning.

The simulator uses finite elements for the discretization of the equations. More details of the code can be found in the following Refs. [8,11,19]. In all the simulated devices, we have considered an undoped substrate ($N_A = 10^{14}\,cm^{-3}$), a metal gate with a work-function of 4.61 eV and an insulator thickness of 1.5 nm. The t_{Si} values considered in our work were 10, 15 and 20 nm.

3. Inversion charge modeling

In this section we propose an analytical model to describe the ICDF of square GAA MOSFETs. As starting point, we used the approach followed by Ge et al. for the symmetrical Double Gate MOSFETs (DGMOSFETs) [20]. Thus, we tried to obtain a 2D analytical model for the ICDF by generalising the 1D eigenfunctions proposed there (Eq. (4) in Ref. [20]). We adapted the quantum mechanical variational calculation employed in [20] for the square geometry corresponding to the GAA MOSFETs considered in this paper, in this way linking the analytical expression of the eigenfunctions to the inversion charge for each gate voltage and device size.

The model obtained with this procedure was compared with the simulation results but it did not fit well for certain gate voltage values and device sizes. The main explanation for this behavior could be the following: the boundary conditions chosen for the electric potential calculation were of Dirichlet kind, using a constant potential value at the semiconductor–insulator interfaces, following the approach presented in [20]. This approximation was good for DGMOSFETs devices because of the one-dimensionality of the structure; however, for a 2D square GAA MOSFETs this is not the case outside the flat band operation regime [8]. More complex boundary conditions would render more realistic results although they would increase the complexity of the analytical models. This extra complexity would make the approach useless from the compact modeling point of view.

Thus, in order to obtain a model analytically simple and accurate enough to reproduce the simulation results for different gates voltages and device sizes, we had to use a different approach. We proceeded to do so by using several trial functions. We found the best results were achieved by making use of the following inversion charge distribution function:

$$f(y,z) = A'\left[\sin\left(\frac{\pi y}{t_{Si}}\right)\right]^{\frac{1}{2}}\left[\sin\left(\frac{\pi z}{t_{Si}}\right)\right]^{\frac{1}{2}}\left(e^{\frac{-b(t_{Si}-y)}{t_{Si}}} + e^{\frac{-by}{t_{Si}}}\right)\left(e^{\frac{-b(t_{Si}-z)}{t_{Si}}} + e^{\frac{-bz}{t_{Si}}}\right) \quad (2)$$

where the normalization of (2) leads to:

$$A' = \frac{\left(1+\frac{b}{\pi}\right)^2 e^b}{t_{Si}\left(b + \frac{b^2}{\pi^2} + \frac{e^b}{2b}\right)} \quad (3)$$

In this way, the electron density can be obtained as $n(y,z) = N_{inv}|f(y,z)|^2$. A heuristic algorithm was developed to determine the value of the b coefficients (i.e., to obtain the dependencies of the b coefficients on the inversion charge and the device size $b(N_{inv}, t_{Si})$). To do this, we calculated and minimized the root mean square error (RMSE) of the simulated and modeled data for the

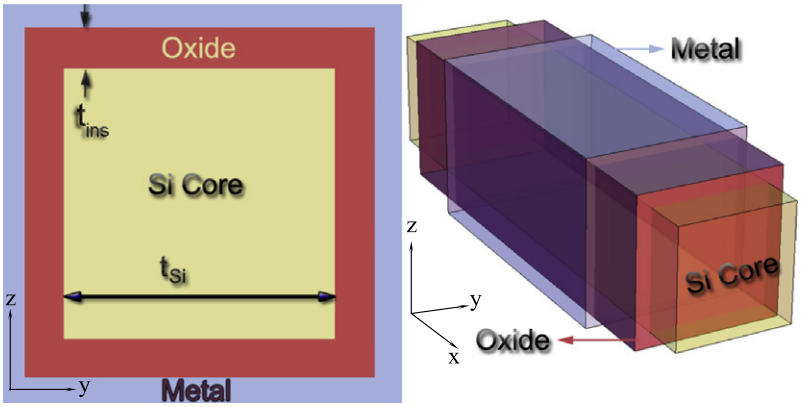

Fig. 1. Cross-section and 3D geometry of the square GAA MOSFETs under study.

inversion charge distribution function for all the grid nodes used in our calculations. The b coefficients obtained are given in Fig. 2 (shown as NA, numerical algorithm). We also developed an empirical analytical expression (4) to reproduce these b coefficients for compact modeling purposes (plotted as FF, fitting function, in Fig. 2). As shown, a good fit is achieved.

$$b = v(t_{Si}) + g(t_{Si})(N_{inv})^{h(t_{Si})} \quad (4)$$

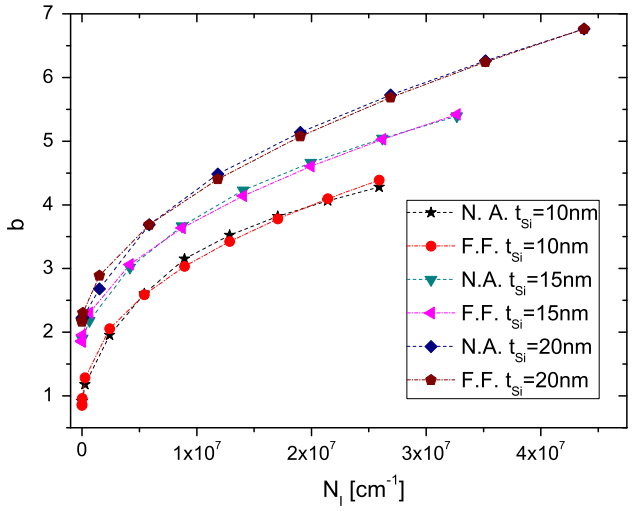

Fig. 2. b coefficients versus inversion charge for different square GAA MOSFETs (t_{Si} = 10 nm, t_{Si} = 15 nm, t_{Si} = 20 nm). The b coefficients correspond to the model proposed in (2). Numerical algorithm (NA) and fitting function (FF) results are shown.

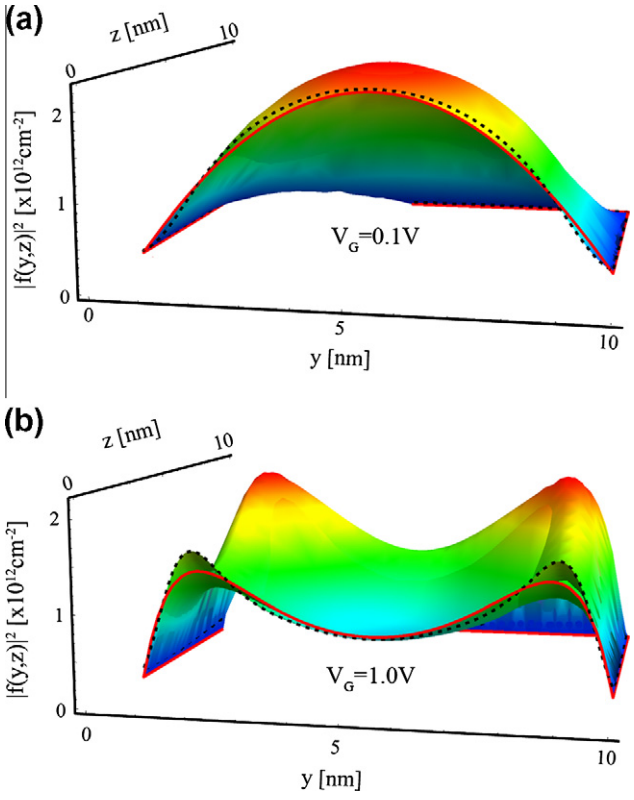

Fig. 3. Three-dimensional view of the inversion charge distribution function for a square GAA MOSFET. The technological parameters used were the following: t_{Si} = 10 nm, t_{ins} = 1.5 nm, $N_A = 10^{14}$ cm^{-3}, $q\phi_m$ = 4.61 eV. The modeled (simulated) data are represented by the surface with solid (dashed) borders. (a) V_G = 0.1 V and (b) V_G = 1.1 V

where

$$v(t_{Si}) = -1.388 \times 10^{12} t_{Si}^2 + 5.481 \times 10^6 t_{Si} - 3.248$$
$$g(t_{Si}) = 2.053 \times 10^9 t_{Si}^2 - 7418.12 t_{Si} + 0.0069$$
$$h(t_{Si}) = -9.353 \times 10^{10} t_{Si}^2 + 376995.66 t_{Si} + 0.1696$$

As can be seen in Figs. 3–5, the new model, despite its relative simplicity, reproduces the simulation data reasonably well. The three dimensional comparison of the simulated and modeled ICDF (the latter obtained with (2)) shows a good fit in Fig. 3. We also analyzed the accuracy of the model in depth by plotting different ICDF cross-sections for several device sizes and gate voltages. In Fig. 4, the t_{Si} = 10 nm device has been chosen and some cross sections of the ICDF are depicted along the y axis for several z values, both in weak and strong inversion. In Fig. 5, ICDF cross-sections are plotted along the y axis for several gate voltages and different device sizes. To obtain the most representative ICDF values (maxima and minima), the selected z positions generally depended on the device size. The fit is good for all the gate voltages considered, as shown in Figs. 4 and 5.

In the following sections, we will use Eq. (2) to approximate the square GAA MOSFET ICDF in order to deal with the ICC and the C_{GC} modeling. As will be shown, the use of more complex models (e. g., a linear combination of eigenfunctions) for the ICDF would make the calculation of the ICC extremely time-consuming.

4. Inversion charge centroid calculation

The ICC in conventional bulk MOSFETs is defined as the first momentum of the inversion charge distribution (the semiconduc-

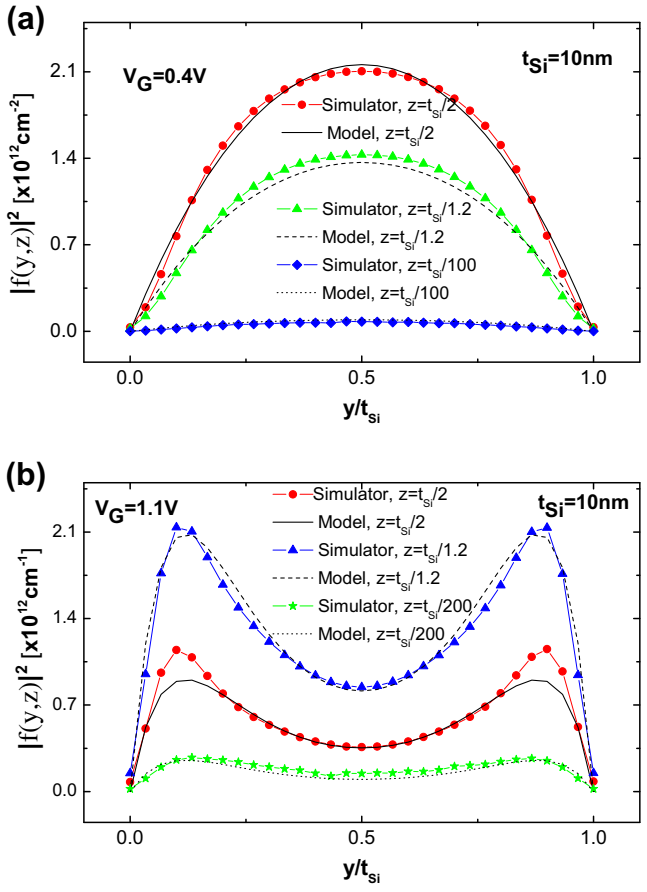

Fig. 4. Inversion charge distribution function cross-sections along the y axis for several z values for a square GAA MOSFET with t_{Si} = 10 nm. (a) V_G = 0.4 V and (b) V_G = 1.1 V

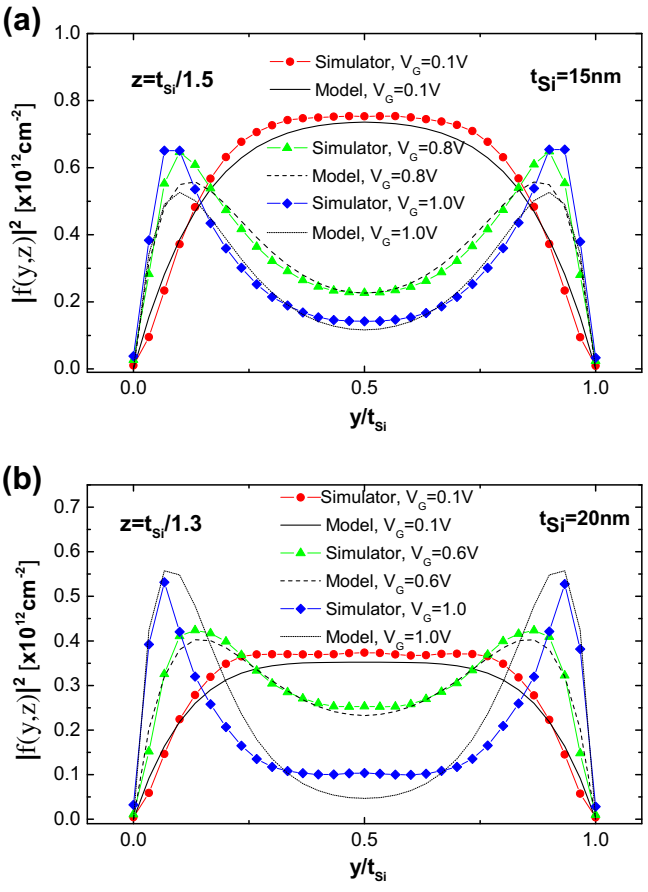

Fig. 5. Inversion charge distribution function cross-sections along the y axis for several gate voltages for square GAA MOSFETs. (a) $z = \frac{t_{Si}}{1.5}$ and t_{Si} = 15 nm. (b) $z = \frac{t_{Si}}{1.3}$ and t_{Si} = 20 nm.

tor–insulator interface is chosen as the origin for this calculation) [21–23]. This parameter is essential in modeling current MOSFETs since when compared to the physical gate insulator thickness, it represents the influence of quantum mechanical effects (QMEs) on the inversion charge spatial distribution. The 1D definition of the ICC is intuitive, as reported in [21–23], and its modeling was carried out in bulk, double-gate and surrounding gate MOSFETs [11,21–23] (note that cylindrical 2D devices can be analyzed as 1D by means of an appropriate choice of coordinate system [11]). However, the definition of a useful ICC for square GAA MOSFETs is not simple. Some attempts towards this definition have been made previously [24,25]. Here, we have followed [25] and dealt with this issue by defining an ideal square (depicted in dashed lines in Fig. 6) with its sides parallel to the semiconductor–insulator interfaces. The sides of the square represent the zones where, on average, most of the inversion charge is placed for a particular gate voltage.

To determine the square that best represents the ICDF, its first momentum $R(\theta)$ has been calculated (here, θ is the angular coordinate of the polar coordinate system with its origin located at the center of the square silicon body, see Fig. 6). The mathematical expression for the $R(\theta)$ calculation is the following:

$$R(\theta) = \frac{\int_0^{\frac{t_{Si}}{2\cos(\theta)}} rn(r\cos(\theta), r\sin(\theta))dr}{\int_0^{\frac{t_{Si}}{2\cos(\theta)}} n(r\cos(\theta), r\sin(\theta))dr} \quad (5)$$

where $\frac{t_{Si}}{2\cos(\theta)}$ is the distance from the center of the silicon core to the semiconductor–insulator interface for each θ value (note that due to

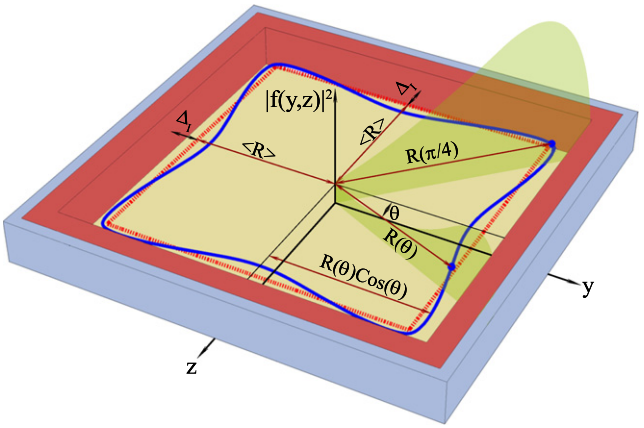

Fig. 6. Representation of the $R(\theta)$ and $\langle R\rangle$ parameters needed for the inversion charge centroid definition of square GAA MOSFETs.

the device symmetry, only $0 \leqslant \theta \leqslant \frac{\pi}{4}$ has to be considered in the calculation of $R(\theta)$).

Fig. 6 shows $R(\theta)$ in solid lines for a square GAA MOSFET. We calculated $R(\theta)$ making use of the ICDF model introduced in the previous section ($n(r,\theta) = N_{inv}|f(r\cos(\theta), r\sin(\theta))|^2$) and compared it with the results achieved using simulated data for all the GAA MOSFETs sizes and gate voltages considered in this work (see Fig. 7). We tried to establish how accurately our ICDF model reproduced the $R(\theta)$ data obtained with simulated data. To do this, we defined an error function, $E_{rr}(\theta)$, as the relative difference between the $R(\theta)$ values obtained with the simulator and with the model:

$$E_{rr}(\theta) = \frac{\Delta R(\theta)}{R_{max}} \times 100(\%) = \frac{|R_{Analytical}(\theta) - R_{Simulator}(\theta)|}{\frac{t_{Si}}{2\cos(\theta)}} \times 100(\%) \quad (6)$$

For each applied gate voltage, we calculated the maximum $E_{rr}(\theta)$ by solving $\frac{dE_{rr}(\theta)}{d\theta}|_{\theta=\theta_{max}} = 0$, and then selected the highest value achieved for each device size. The results are summarized in Table 1. As can be seen, the model also works well (in relation to the calculation of $R(\theta)$) for all the devices under study and for the whole bias voltage range considered.

To calculate the size of the ideal square that models the inversion charge position (see Fig. 6), the geometric average of the $R(\theta)$ projection at the Y axis was estimated as:

$$\langle R\rangle = R_I = \left(\prod_{k=0}^{N}\left[R\left(\frac{k\pi}{4N}\right)\cos\left(\frac{k\pi}{4N}\right)\right]\right)^{\frac{1}{N+1}} \quad (7)$$

Finally, the average inversion charge centroid, Δ_I, was calculated as is usual in 1D MOSFETs, i.e., by considering the origin to be at the semiconductor–insulator interface. This definition (see the equation below), which makes use of R_I, allows the inclusion of QMEs in the gate capacitance model as will be shown in the next section.

$$\Delta_I = \frac{t_{Si}}{2} - R_I \quad (8)$$

The Δ_I data are plotted in Fig. 8. It can be seen that the ICC values obtained with the simulation results correctly reproduce those calculated using the ICDF model (2).

5. Gate-to-channel capacitance modeling

The gate-to-channel capacitance, C_{GC}, is an essential MOSFET parameter since it determines the transconductance of the transistor [2,10]. In 1D devices, C_{GC} can be calculated as the series

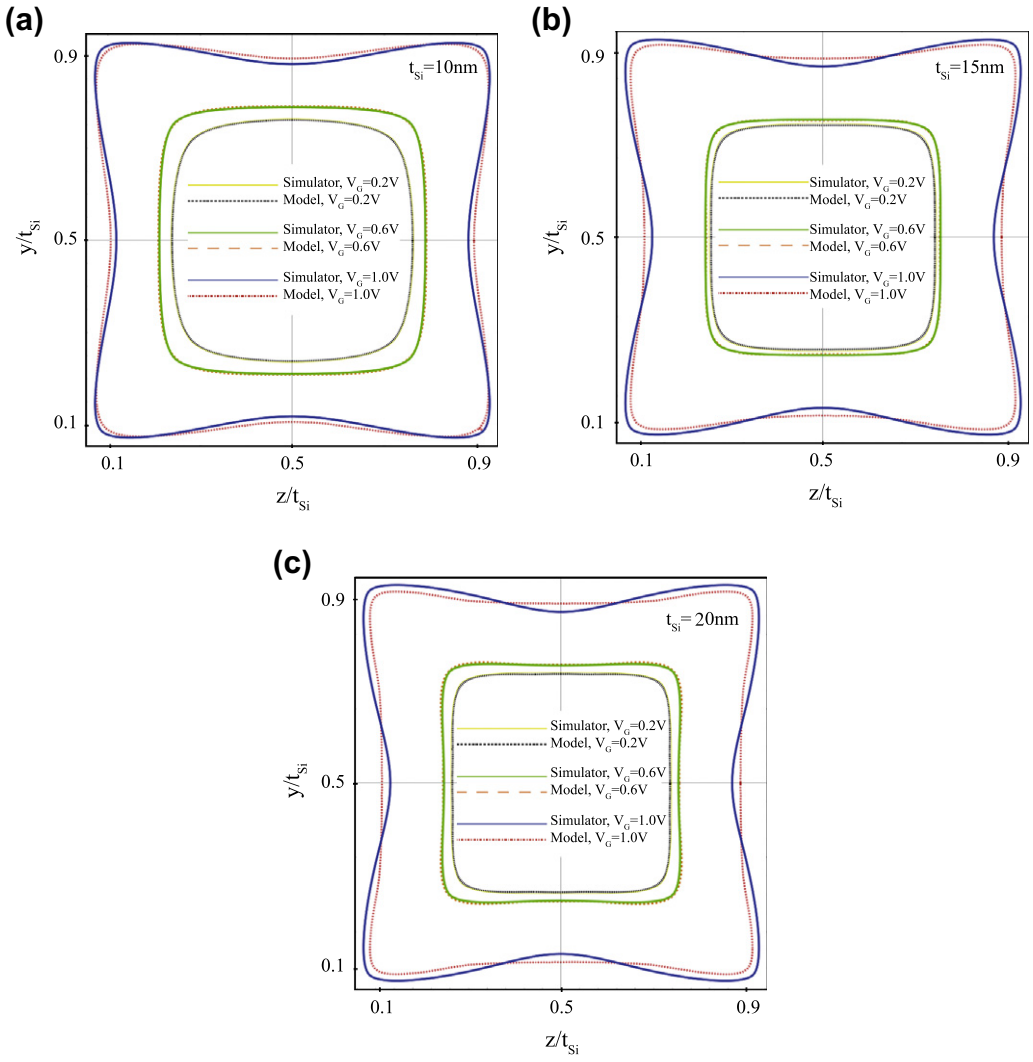

Fig. 7. $R(\theta)$ polar plots for square GAA MOSFETs. The inversion charge centroid is calculated with modeled and simulated data for several V_G voltages. (a) t_{Si} = 10 nm, (b) t_{Si} = 15 nm, (c) t_{Si} = 20 nm.

Table 1
Maximum value of the $E_{rr}(\theta)$ function for the GAA MOSFETs studied.

t_{Si}	10 nm	15 nm	20 nm
E_{rr}^{MAX}	1.6 %	3.5%	4.6%

combination of the gate insulator capacitance C_{ins} and the channel capacitance C_{ch} [26–29]:

$$C_{GC} = \left(\frac{1}{C_{ins}} + \frac{1}{C_{ch}}\right)^{-1} \tag{9}$$

However, in the case of square GAA MOSFETs, several approximations are needed to achieve our goal of developing a simple analytical expression for C_{GC}. First, the semiconductor–insulator interface is not isopotential, making Eq. (9) an approximate expression [8,19,25]. Moreover, there are no closed analytical expressions either for C_{ins} or for C_{ch}. For the insulator capacitance term, an empirical expression previously obtained by curve-fitting was used [30]:

$$C_{ins} = \frac{5\epsilon_{ins}}{\ln\left(1 + \frac{5t_{ins}}{4t_{Si}}\right)} \tag{10}$$

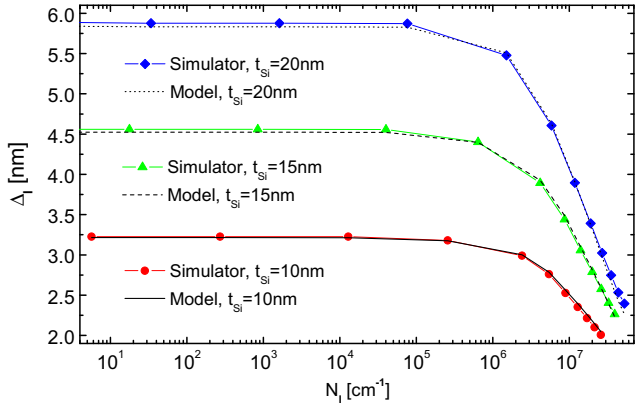

Fig. 8. Average inversion charge centroid versus inversion charge for square GAA MOSFETs of different sizes.

It can be seen that for low values of the t_{ins}/t_{Si} ratio (within the limit $t_{Si} \gg t_{ins}$), the C_{ins} value of a conventional bulk MOSFET is obtained, as should be the case.

Regarding the channel capacitance, an approximate expression can be achieved, using the expression corresponding to DG MOSFETs, which can be calculated as:

$$C_{ch}^{-1} = \frac{d\phi_s}{dQ_{inv}} = \frac{d(\phi_s - \phi_c)}{dQ_{inv}} + \frac{d\phi_c}{dQ_{inv}} \quad (11)$$

ϕ_s and ϕ_c being the electrostatic potential at the surface and the center of the silicon body, respectively, and Q_{inv} the inversion charge per unit length ($Q_{inv} = qN_{inv}$). The former equation can be rewritten as [31,32]:

$$C_{ch}^{-1} = \frac{x_i}{W\varepsilon_{Si}} + \frac{Q_{inv}}{W\varepsilon_{Si}}\frac{dx_i}{dQ_{inv}} + \frac{d\phi_c}{dQ_{inv}} = \frac{1}{C_{inv}} + \frac{1}{C_c} \quad (12)$$

where x_i is the charge centroid position, defined in [22], and W is the transistor width (necessary to calculate the capacitance per unit length). A description of the physical meaning of each of the capacitance terms can be found in [32].

In order to model the gate capacitance of square GAA MOSFETs, a term equivalent to each of (12) is needed. First, a model of the electric potential within the silicon body is needed to calculate C_c. Due to the lack of symmetry of this kind of device, an alternative option is to make use of the similarities found between the potential behavior in cylindrical and square GAA devices [33]. An example of these similarities is found in Fig. 9, where $d\phi_c/dQ_{inv}$ is compared for cylindrical and square GAA MOSFETs. As can be seen, the results for the two devices are found to be almost identical. Analytical models for the electrostatic potential of cylindrical GAA devices are available in the literature [9,34,35], and here we have modeled the potential at the center of a square GAA MOSFET making use of the expression proposed in [9]. Thus, the C_c term can be calculated as [32]:

$$C_c = \frac{Q_0 k_B T}{qQ_{inv}(Q_0 + Q_{inv})} \quad (13)$$

where $Q_0 = (k_B T/q)8\pi\varepsilon_{Si}$ and the remaining parameters keep their usual meaning.

To calculate the inversion capacitance term in (12), C_{inv}, the DG centroid definition was first replaced by the one introduced in this work for the square GAA device. Then, the planar capacitance formula $W\varepsilon_{Si}/x_i$ was replaced by its square quadruple-gate counterpart (found from (10) where t_{ins} and t_{Si} are replaced by Δ_I and $t_{Si} - 2\Delta_I$, respectively). Finally a fitting parameter F replaced the channel width W in the second part of the C_{inv} term, to appropriately take into account the 2D confinement effect. The resulting expression for square GAA MOSFETs C_{inv} is:

$$C_{inv}^{-1} = \left(\frac{5\varepsilon_{Si}}{\ln\left(1 + \frac{5}{8}\frac{\Delta_I}{R_I}\right)}\right)^{-1} + \frac{Q_i}{F\varepsilon_{Si}}\frac{d\Delta_I}{dQ_{inv}} \quad (14)$$

For the sake of compactness, we have developed an empirical expression to obtain the values needed for the F parameter as a function of t_{Si} (here, both t_{Si} and F are given in centimetres):

$$F = 2.9 \times 10^{-6}\ (\text{cm}) - 4.45 t_{Si} + 2.9 \times 10^{6}\ (\text{cm}^{-1}) t_{Si}^2 \quad (15)$$

Fig. 10 shows the overall gate capacitance obtained from the simulation of a square GAA MOSFET with $t_{Si} = 10$ nm, and each one of its components (i.e., C_{ins}, C_{inv} and C_c), calculated using the models developed. As can be seen, the C_c term controls the behavior of the device in the weak inversion regime, while C_{inv} is responsible for the gate capacitance degradation with respect to the ideal limit value C_{ins}. A very good agreement between the model and the simulated data is achieved.

We have compared the simulated gate-to-channel capacitance values with those obtained with (9) for various device sizes and the results are plotted in Fig. 11. As can be seen, quite a good fit is achieved in both the weak and strong inversion regimes. It should be highlighted that the different capacitances obtained with (9), plotted in symbols, were calculated through a fully analytical

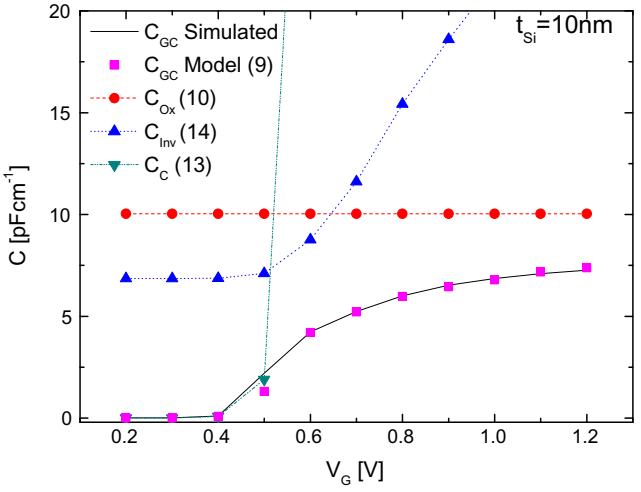

Fig. 10. Decomposition of C_{GC} versus V_G for a GAA MOSFET with $t_{Si} = 10$ nm into its three components: C_{ins}, C_{inv} and C_c.

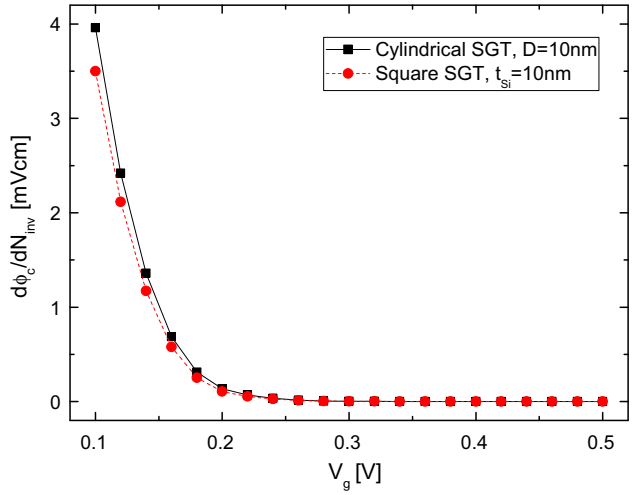

Fig. 9. Comparison of $d\phi_c/dN_{inv}$ for cylindrical and square GAAs with $t_{Si} = 10$ nm and $D = 10$ nm, respectively.

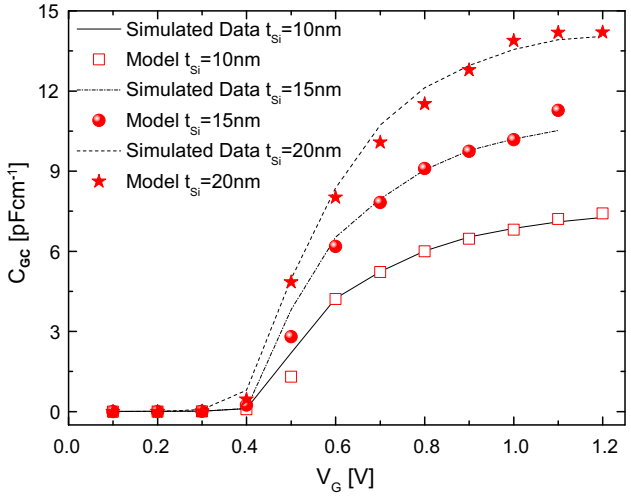

Fig. 11. C_{GC} versus V_G for GAA MOSFETs of different sizes: results for $t_{Si} = 10$ nm, $t_{Si} = 15$ nm and $t_{Si} = 20$ nm are included. The simulated (modeled) data for the capacitance are shown in solid lines (symbols).

approach, which involved the calculation, using (2), of the ICDF for each device size and gate voltage, and the subsequent estimation of Δ_I making use of (8). Therefore, the model introduced in this work reproduces reasonably well the simulation data obtained for the inversion charge distribution, the charge centroid and the gate-to-channel capacitance for different device sizes and bias voltages.

6. Conclusions

We have introduced an analytical model for the inversion charge distribution function of GAA MOSFETs where quantum effects have been taken into account. The model has been tested by means of a comparison with simulation data obtained by self-consistently solving the 2D Schrödinger and Poisson equations for a wide variety of device sizes and bias ranges.

We have also calculated the inversion charge centroid and gate-to-channel capacitance by using the inversion charge distribution function developed previously. A very good agreement between the simulated and modeled data was achieved both for the ICC and the C_{GC} for different device geometries and biases. The simplicity and accuracy of the models presented are very promising from the compact modeling point of view since GAA MOSFETs are considered good candidates for future sub-22 nm integrated circuit technologies.

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